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Have Your Cake and Eat It, Too: Engineering Measurements at Fabrication for Channel Design and Process Control

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DesignCon 2014

Have your cake and eat it, too: Engineering measurements at fabrication for channel design ***and*** process control

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Abstract

This paper demonstrates the acquisition of advanced circuit board performance parameters from breakaway test coupons measured right at the PCB fabricator. We show how to acquire S-parameter and TDR-based measurements up to 30 GHz using robust probes and test coupon fixtures. The measurements provide pass/fail tests for process control *and* they provide model parameters as feedback to improve channel design. By way of example, we demonstrate measurements of several representative test coupons, perform total loss tests, such as SET2DIL, and extract design parameters that can be used to improve EDA channel models. We also demonstrate measurement and tests of impedance uniformity and differential delay skew, both of which are influenced by glass weave position and copper fabrication variations. Archiving fundamental S-parameter and TDR measurements allows for further extraction of important design-to-fabrication feedback while in the process of tracking PCB process statistics.

Authors Biography

Dr. Don DeGroot operates CCN (www.ccnlabs.com), a test and design verification business he co-founded in 2005 to support high-speed electronic design. Don has over 25 years experience in high-frequency electrical measurements and design, including his PhD degree from Northwestern University and 12 year of research at NIST. Don currently focuses on interconnection and PCB material characterization for serial data applications.

Bret Moreland is a test and measurement engineer working in the data storage industry since 1986. He has developed automated test systems used in manufacturing test of printed circuit boards and hard drive assemblies for MiniScribe, Maxtor, and Cornice. Bret is currently a test engineer at CCN, characterizing printed circuit board materials and interconnects used in high-speed serial designs.

Dr. Eric Bogatin received his BS in physics from MIT and MS and PhD in physics from the University of Arizona in Tucson. He has held senior engineering and management positions at Bell Labs, Raychem, Sun Microsystems, Ansoft and Interconnect Devices. Eric has written 6 books on signal integrity and interconnect design and over 300 papers. His latest book, Signal and Power Integrity- Simplified, was published in 2009 by Prentice Hall. He is currently a signal integrity evangelist with Bogatin Enterprises, a wholly owned subsidiary of Teledyne LeCroy. He is also an Adjunct Associate Professor in the ECEE department of University of Colorado, Boulder. Many of his papers and columns are posted on the www.beTheSignal.com web site.

Introduction

Multigigabit channel design requires feedback from measurements of fabricated test lines to optimize EDA input parameters and channel models. Quantifying variation in materials, glass-weave, and fabrication is key. Test systems with robust probes and fixtures can acquire this design feedback from production test coupons while at the same time providing pass/fail testing for process control. The key is to measure S-parameters on the factory floor and to extract the model parameters by analysis. In this way both the designer and the manufacturer receive valuable feedback for improving serial channel performance.

Recent DesignCon papers [1-3] provide the basis for describing channel loss in terms of effective model parameters: an effective permittivity for the dielectric and at least two effective resistivity parameters for the copper foils. These effective parameters are used in computer-aided design tools to correctly predict loss vs. frequency and to optimize transmission line design for a given set of dielectric and copper foils. While the effective material parameters are difficult to obtain from physical profile measurements alone, electrical measurements can be used to obtain the effective parameters, leading to a measurement-based design that is more representative of a given PCB stack-up and specific manufacturing line.

Acquiring measurements on PCBs that directly tie production to design has remained a challenge. Engineers create and fabricate test boards prior to production in order to verify and adjust channel models, but these test boards may not be exact representations of production boards, so they cannot be used to predict channel performance changes with production variation. Unless an extensive number of test boards were created, the channel models and material parameters extracted from the pre-production tests will not capture the likely variance of production.

Further, since fabricators have relied on impedance testing for PCB production control, we have not been able get high-frequency scattering parameters on critical path transmission lines during active PCB production; we've had to test samples with some amount of delay outside of the production environment.

Now, with the continued push to use total signal loss [4-8] as the means of verifying PCB production for multigigabit channels, there is an opportunity to locate high-frequency network analysis instruments and fixtures in production environments. These systems not only afford the important process controls of total loss, but also provide access to engineering feedback parameters and statistics through S-parameter and TDR measurements approaching 30 GHz.

Reference methods for acquiring accurate transmission line parameters rely on TDR or VNA measurements of two or more transmission lines that differ in length only [5,7]. For differential line testing, this requires 4-port measurements of multiple lines. Implementations of the SET2DIL production test method [4] get by with 2-port connections, but require measurements of a "THRU" device and a shorted transmission

line device (Fig. 1). While an engineering lab may not object to multiport measurements of multiple devices, production test labs do object.

The goal is to acquire as many transmission line parameters as possible from S-parameter measurements of a single test. Last year, Pupalaikis and Doshi [8] described the theory and application of frequency-domain analysis to differential scattering parameters of the SET2DIL test devices. Here we show a system for production testing that acquires a number of key transmission line parameters from a single SET2DIL-like test. The system approach includes calling any test algorithm used in practice, but we use simulation and test examples below to explain the process of taking two-port measurements of a single SET2DIL-like test device.

Equipped with such reduced measurements, engineers and fabricators can quickly access propagation loss statistics, estimates of dielectric and copper loss, impedance variation over line length, differential delay and loss skew, and changes in line coupling. This is in stark contrast to making multiple measurements to perform only a single test.

All this information can be used to optimize the channel, hedge against practical production variation, and provide guidance to material suppliers and fabricators in prioritizing variance control.

A key feature of this new test strategy is that the same SET2DIL-like test structure measured from coupons on the production floor to indicate pass or fail condition, can also be used in an R&D environment to extract more detailed performance information.

The wealth of information is there for the taking, and the designers that make use of it can get their products manufactured to a tighter spec, and simultaneously improve their design models (that's the source of the "have your cake and eat it, too" idiom).

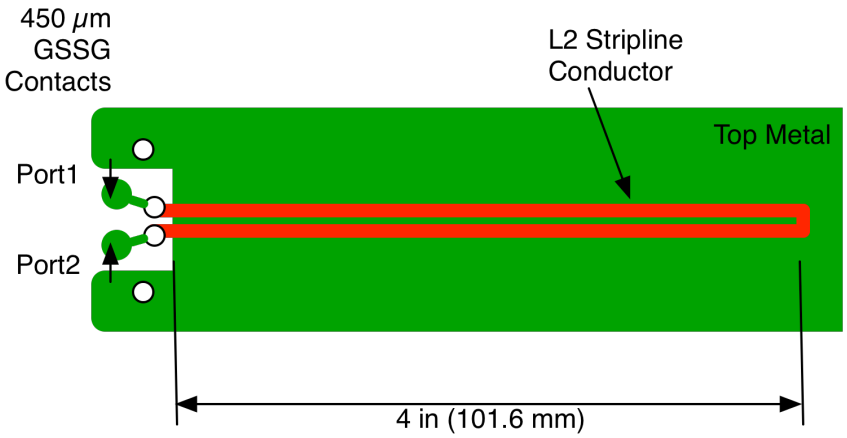

Fig. 1. Two-port stripline test device based on SET2DIL [4]: segment of uniform differential transmission line with differential short circuit and common mode open circuit at far end.

Method

We focus on the measurements of SET2DIL-like test structures [4] but interpreted slightly differently than the conventional approach. Figure 1 shows that the test structure is a length of differential transmission line, with the far end shorted differentially but with open-circuit common mode. These test structures are measured with connections at one end only.

In the current method discussed here, we interpret this structure as a single differential pair with single-ended port connections at one end. The single-ended S-parameters can be measured with a 2-port network analyzer working in the frequency or time domain.

There are five steps in the analysis of the S-parameter measurements:

1. measure the 2-port S-parameters at the near end of the shorted differential pair

2. de-embed the launch to arrive at the S-parameters of the uniform differential pair

3. convert the single ended S-parameters into differential S-parameters

4. extract the important performance parameters:

    a. differential impedance
    b. common impedance
    c. differential insertion loss
    d. differential time delay
    e. effective dielectric constant
    f. mode conversion

5. analyze and interpret the results

To illustrate the process and identify the features to expect from real systems, we first apply this process to simulated data. A simple, ideal tightly coupled stripline differential pair model was built in simulation with a spacing equal to the line width. The single ended impedance was designed to be slightly off from 50 Ohms, with differential impedance near 90 Ohms. The simulations and display of the data were done with Agilent's ADS.

To further facilitate the analysis of this measurement method, we simulated the complete 4-port single ended S-parameters from this ideal differential pair, from which it is easy to extract all the useful performance figures of merit (FOM). Where appropriate, the 4-port values are compared with the 2-port values.

In the model data from the simulated ideal differential pair, Steps 1 and 2 are skipped since the simulated single-ended S-parameters are the S-parameters of just the uniform part of the DUT.

Step 3

In this step we start with the single-ended S-parameters of the uniform differential pair, shorted at the far end. It is always a good policy to anticipate what to expect and then compare to the actual result.

It is easy to anticipate the S-parameters when displayed in the time domain with a step response. The single-ended TDR response, S_{11} in the time domain, will be related to the mismatch of the impedance of the line and the port impedance.

The S_{21} term in the time domain will be the near end cross talk. In the case of tightly coupled striplines, this will be on the order of 6%.

Figure 2 shows the single-ended TDR response and near end S_{21} for the tightly coupled pair simulated for the 2-port approach and the 4-port approach. The single-ended characteristic impedance of the line, 52.3 Ohms, is the same in both approaches. Likewise, the near end cross talk, roughly, 6%, is the same in both approaches. These results are reasonable and expected.

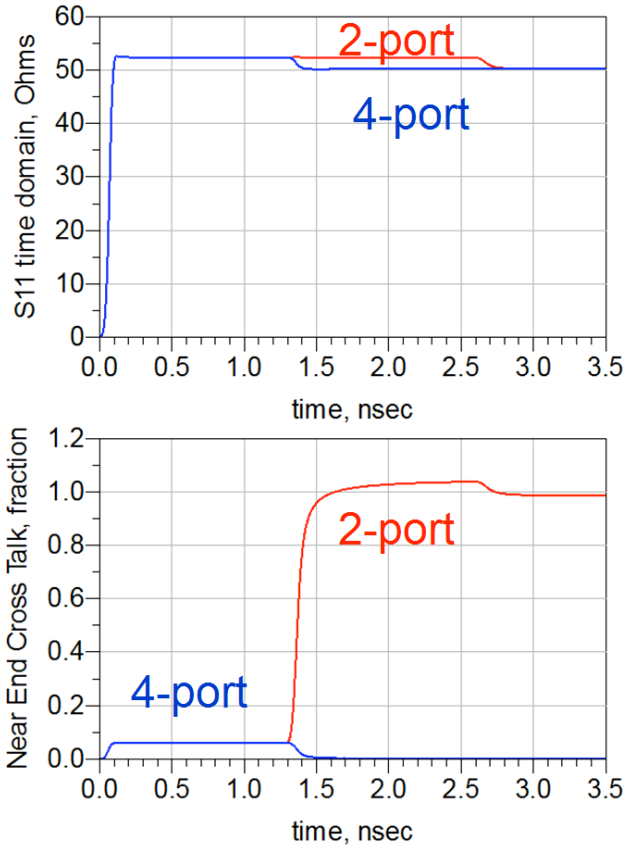

Fig. 2. Simulated single-ended time-domain response for example differential pair: 2-port test device and matching 4-port line.

This step involved converting the single-ended S-parameters into the differential S-parameters. This is done using conventional matrix algebra, with the condition that for the 2-port file, all we can extract will be the differential matrix elements looking from differential port 1. This will include S_{DD11}, S_{CC11} and S_{CD11}.

Of course, in the case of the 2-port structure, the far end has a differential short, while for the 4-port case, the far end has a 100 Ohm differential termination. While the S_{DD11} for these two examples will look very different in the frequency domain, they should offer the same differential impedance in the time domain. Figure 3 shows the simulated differential return losses from the two examples in both the frequency and time domains. The differential impedance of the pair can be read off the screen directly as 97.8 Ohms.

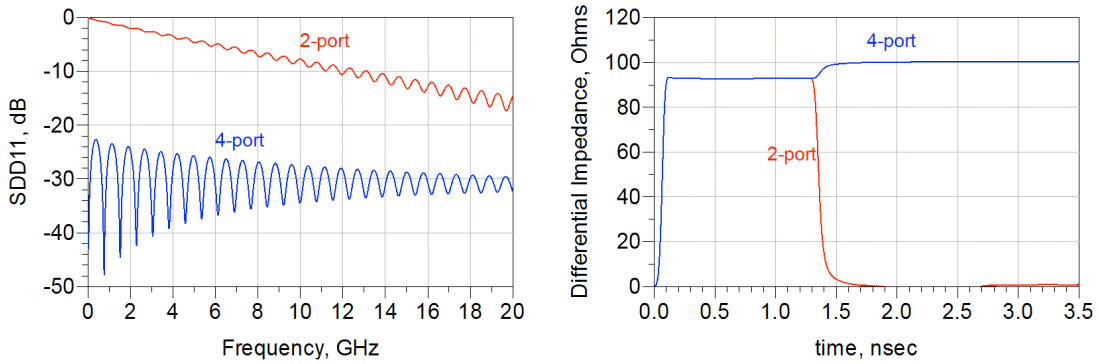

Fig. 3. Simulated differential response for example differential pair: 2-port test device and matching 4-port line.

Since the two lines simulated are identical, there is no mode conversion and S_{CD11} is a large negative dB value, with no significance in this simulated example. While the S_{CC11} term provides information about the common impedance of the differential pair, it is not important in this analysis.

Step 4

In the two-port test structure, with a differential short at the far end, the differential return loss looks like a differential insertion loss. This is not a coincidence.

The return loss is really due to signal propagation down the line, a reflection at the short, where the phase is advanced by 180 degrees, and a propagation back to the source. The propagation down and back on the line is equivalent to the S_{DD21} for an 8-inch long interconnect with 180 degrees phase advance on reflection. We can write the S_{DD21} for an interconnect twice as long as the test line as:

$$SDD21_{2x} = (-1)\,x\,SDD11$$

In this equation the (-1) rotates the phase back 180 degrees to compensate for the phase shift on reflection. The 180 degree phase shift is (-j) x (-j) = (-1). This is the differential

insertion loss for a line that is twice the actual length. The magnitude and the phase of the differential insertion loss will correspond to a line that is twice the test line's length.

From the time domain, we have shown how we can get the single-ended and differential impedance of the lines. We also get a good metric of the uniformity of the lines. After all, an important assumption in the analysis of this measurement is that the impedance of the lines is constant.

From the differential insertion loss, we can calculate the total attenuation, and from the phase, the time delay, and from the time delay and the length, the effective dielectric constant.

The differential insertion loss per inch from these two ideal models, are plotted in Fig. 4. They should be identical. Also plotted is the phase for the differential insertion loss. Since the phase of the S_{DD21} from the 2-port case is actually equivalent to an 8-inch long differential pair, the phase will advance twice as fast as for a 4-inch long pair. This is seen in the results.

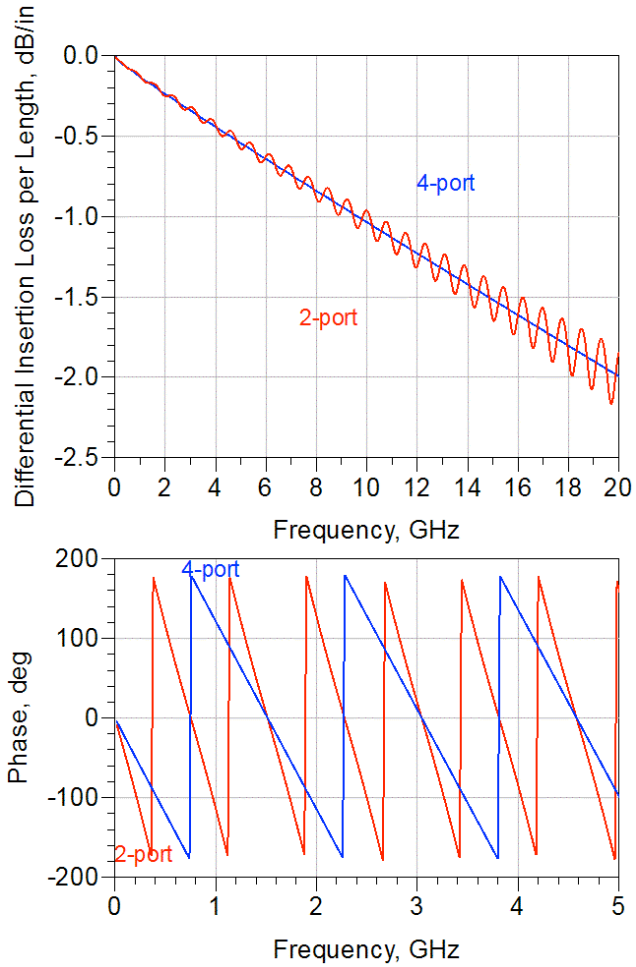

Fig. 4. Simulated differential insertion loss for example differential pair: 2-port test device and matching 4-port line.

The excess ripple in the differential insertion loss is from the impedance mismatch between the port impedance and the line impedance. Since the differential insertion loss for the 2-port case is really derived from the differential return loss, it is more sensitive to reflections. However, this can be reduced considerably by re-normalizing the differential port impedance to the differential characteristic impedance of the pair, as indicted in the TDR response. This was 92.8 Ohms. Figure 5 shows the re-normalized differential insertion loss per inch for the two cases, with two different port impedances.

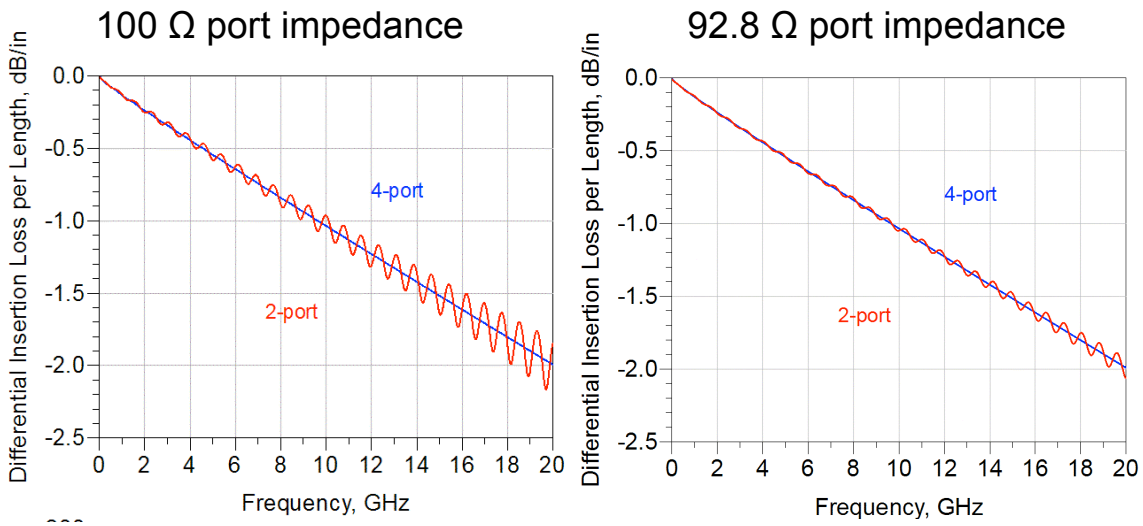

Fig. 5. Simulated differential insertion loss for two port impedance normalizations, extracted from example differential pair: 2-port test device and matching 4-port line.

There is still a residual amount of ripple in the derived differential insertion loss for the two-port device. It is interesting that the differential loss of the four-port method goes through the middle of the ripples on the dB scale, suggesting an interpretation. No amount of optimizing the port impedance, if using only a real impedance value, will totally reduce the ripple in the differential insertion loss. However, it will condition the insertion loss so the ripple is symmetric about the true four-port response.

In these examples, the port impedance used was a real value, when, in fact, the differential impedance is complex-valued, due to the losses in the line:

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}.$$

The next phase of this program will explore re-normalization using the complete complex port impedance following [7].

From the phase of the differential insertion loss, we can calculate the time delay for the differential signal, as

$$TD = \frac{\text{unwrapped}(\text{phase}(SDD21))}{\text{frequency}}$$

From the time delay of the interconnect, and its physical length, we find the effective dielectric constant, as

$$Dk_{eff} = \left(\frac{c}{v}\right)^2 = \left(c\frac{TD}{Len}\right)^2$$

This effective Dk assumes, to first-order, that all dispersion is from the dielectric material and none is from the frequency dependence of the current distribution affecting the inductance of the conductors.

For the two-port test device, the effective length of the test line is 8 inches, since the differential insertion loss is a round trip value; for the equivalent four-port line, the length is the one-way trip. Figure 6 shows the extracted differential time delay and the extracted effective dielectric constant for the two test cases. Of course, the time delay for the 2-port example will be longer, since it corresponds to a round trip distance. However, both approaches offer exactly the same effective dielectric constant.

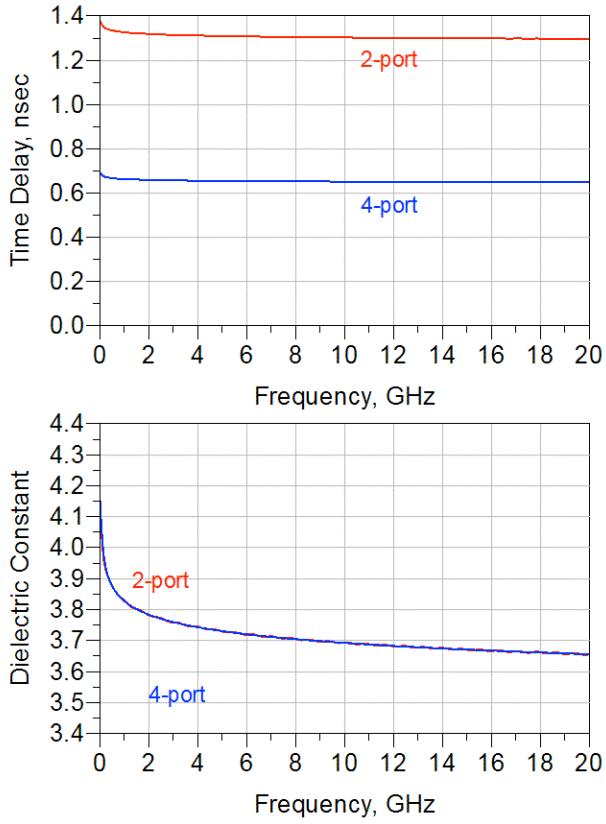

Fig. 6. Propagation delay and effective dielectric constant extracted from simulated differential pair: 2-port test device and matching 4-port line.

In the simulated model, a value of 3.8 was used as the dielectric constant at 1 GHz. The simulator uses a wide band Debye model for the dielectric constant, which shows as a slight dispersion.

Step 5

The final step is analysis of the results. This approach of interpreting the SET2DIL test structure as a differential pair with a differential short at the end, results in more than just a total loss measurement.

From the time domain display of S_{DD11}, we get the differential line impedance.

From the measured S_{DD11}, we get the differential insertion loss per length, the propagation delay and the effective dielectric constant.

Using a 4-port simulation of the same structure, we compared line parameters extracted from the measurements of the two-port test device with the reference 4-port values and found them to be identical. This illustrates the technique proposed here can extract the intrinsic properties of the fabricated transmission line. All of which are suitable for production testing, and as feedback into design models that need to predict the performance of the fabricated channel.

The one important residual artifact is a slight amount of ripple in the insertion loss, due to a very small impedance mismatch between the real port impedance and the complex characteristic impedance of the line.

In the 2-port case, the ripples in the insertion loss are due to the interference between the reflection off the front interface between the line and the port, and the reflection off the short at the far end. This is first order with the reflection coefficient.

In the 4-port case, the ripple in the insertion loss would be due to the interference between the first pass transmitted signal, and any further reflected signals, which would have to reflect off of two interfaces to get back to the far end port. This ripple would be related to the square of the reflection coefficient at one interface.

If the reflection coefficient were on the order of 2%, due to the imaginary component of the characteristic impedance, this would be a 2% ripple effect for the 2-port case and a 0.04% effect for the 4-port case, which is why we don't see it. This analysis also points out how important the slight mismatch at the launch of the line is to contributing to ripple, and ultimately the irreproducibility of the insertion loss due to very small changes in the probe contacts to the test coupons.

A launch with excess inductance or capacitance from features in the pad stack or irreproducible alignment from manually probing, will contribute to more ripple, even in the best case.

Measurement Demonstration

We fabricated test coupons with two-port SET2DIL-like test lines (Fig. 1) and matching four-port differential lines. We included both microstrip and stripline devices. We used a range of PCB materials, including advanced FR4 materials with higher-performance glass. The purpose of having both SET2DIL-like test lines and full four-port differential lines is to compare the extraction of transmission line parameters to actual differential parameters. We follow the five steps outlined above to arrive at a number transmission line parameters and tests starting from two-port measurements of the SET2DIL-like test device.

Step 1: Two-Port S-Parameter Measurements

In order to achieve repeatable high frequency measurements, we used a 30 GHz production test fixture (nTegrity) connected to a 40 GHz time-domain network analyzer (SPARQ) as shown in Fig. 7.

Small variations in signal launch admittance can have deleterious effects on measurements after de-embedding, including the introduction of non-causal and non-passive behavior. To avoid these, we used a production test fixture that provides repeatable alignment and clamping pressure, pressing the test coupon onto robust electrodes without the problems of holding a probe by hand (Fig. 8). The production test fixture pins and electrodes match the pads and alignment holes of the SET2DIL method.

We also examined results using GSSG microprobes. The probes were hand-held types made for the SET2DIL test coupons (Fig. 9). They were connected to the SPARQ using the manufacturers test port cables. In our testing, we clamp the probes to the test coupon using a low cost probe station in order to achieve good launch performance and repeatability.

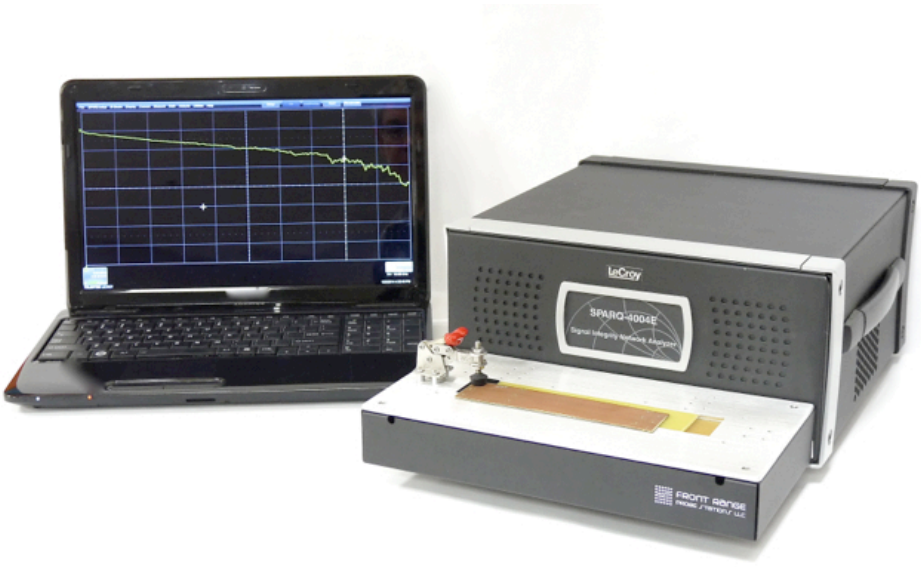

Fig. 7. Production test system (nTegrity) showing fixture and time-domain network analyzer (SPARQ).

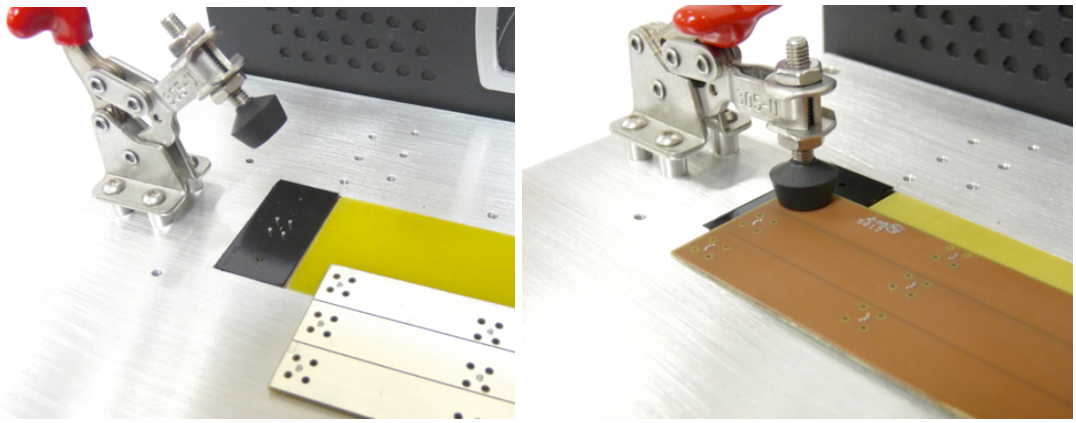

Fig. 8. nTegrity test coupon fixture showing robust electrodes, test coupon, and test coupon clamped onto alignment pins and signal electrodes.

Fig. 9. Bottom view of the delicate tips of a 450 µm GSSG SET2DIL probe (handheld).

Contact Schemes

The demonstration includes PCB test coupons with the pads specified by the SET2DIL method, and coupons using modifications (while holding the same spacing). We had identified differences in S-parameter measurement performance for different probe and fixture connections, and in the process, dramatically improved the "transparency" of the nTegrity-to-device transitions by modifying the location of the ground vias and the ground surrounding the signal pads at the coupon launch points.

A close up of two launch footprints are shown in Figure 10 along with the time-domain impedance responses of the launches as seen by three different probes and the nTegrity test fixture. One launch structure is the recommended Intel SET2DIL landing pattern. Here there is a significant distance between the location of the return vias for the underlying return planes, and the launch point. In addition, there is a long path between the contact pads and the signal vias for the buried signal traces.

These increased distances have the effects of: 1) adding an inductive discontinuity at the signal via location; and 2) increasing the coupling between the probe-to-launch structure. This means that coupling in the launch must be taken into account when de-embedding the test device response from the raw measurement.

The improved launch footprint reduces the impedance discontinuity of the launch. This helps both de-embedding (Step 2) and measurement repeatability due to smaller Z(d) derivatives. For the examples included in this study, the modified pad structure was used.

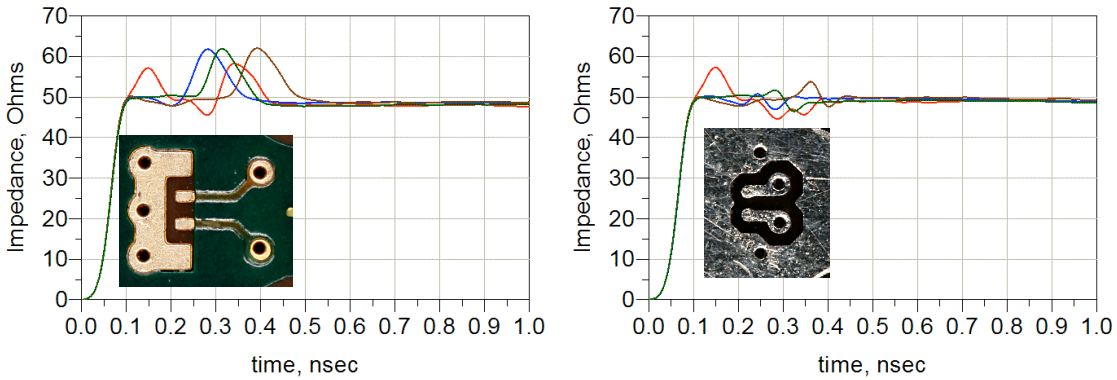

Fig. 10. Footprints and impedance profiles of the as-specified SET2DIL pads (left) and modified pads (right).

It should be noted that due to the nature of the fringe fields at the interface of the pads and probes electrodes, some probes may be more transparent for a given pad structure, and others not so much. From the probe-pad examples above, we see that adjusting the location of the return via in the launch will affect the quality of the launch in different ways for the different contacts. Launch footprints must be matched to the particular probes to optimize de-embedding and repeatability; a follow on project will seek to optimize the design of the launch even better.

Two-Port Measurements

The high-frequency measurements cannot be discussed without first emphasizing the importance of ESD protection for time-domain network analysis. Even if the user is grounded to the instrument through good practice, the test coupon conductors will likely be storing electrostatic charge at a significant potential. The nTegrity system uses the built in port-switching network of the SPARQ to hold the coupons in a discharged state during mounting and un-mounting, and it only makes connection to the sensitive pulser/sampler during the short period of the electrical measurements (hands away).

The network analyzer was calibrated to the end of the 2.92 mm coaxial test port cables using traditional vector network analyzer methods. The frequency range of the calibration exceeded DC-30 GHz. The test fixture transitions were attached at this calibration reference plane. The two-port test devices were placed on the fixture electrodes using the alignment pins and holes, and clamped into place.

Automation software initiated the acquisition of the two-port calibrated S-parameters. The calibrated S-parameters are stored to disk.

At this point, the two-port measurements are not very useable since they include the effects of the transition from the calibration reference plane to test line, the mismatch between Z_0 and the port impedance, and the effects of the right-angle bends of the far-end differential short circuit (see Fig. 11). We could not easily test fabricated line performance using this data alone.

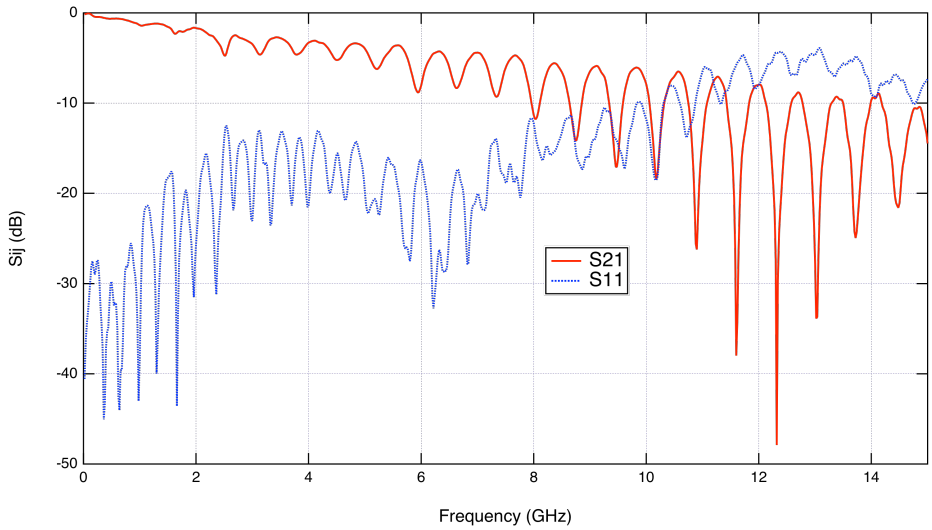

Fig. 11. $|S_{21}|$ *and* $|S_{11}|$ *of the two-port test device attached to the nTegrity fixture. Sij referenced to the calibration reference plane and impedance without de-embedding.*

Step 2: De-embedding

To remove the imperfections of the probe and/or fixture, we have to move the reference plane to the beginning of the uniform, coupled transmission line. This means de-embedding the interconnections from the end of the coax to the beginning of the test line.

There are a variety of ways of de-embedding [9]. For example, if a 2x thru calibration structure is fabricated adjacent to the test structure, it's possible to build an S-parameter file for the launch and to correct the measurements with linear algebra. This is the technique implemented in Agilent's Automatic Fixture Removal (AFR) algorithm, as an example.

Alternatively, the Teledyne LeCroy Peeling Algorithm builds the S-parameter model for the launch *in-situ* from the time-domain measurements of the launch-to-test device path. This requires knowing the precise time delay from the end of the coaxial calibration reference plane to the beginning of the uniform transmission line of the test device.

The time delay is accurately determined directly from the S_{21} TDT response. For the SET2DIL-like test devices, this is the near end cross talk. The time at which the near end cross talk turns on is exactly the round trip time from the end of the coax where the

reference plane ends, to the beginning of the coupled region of the differential pair. At this location the electromagnetic fields are mostly transverse to the propagation direction and no other electromagnetic modes persist. For the nTegrity fixture, we identify the time delay to the beginning of the launch to be about 180 psec.

We saw in our simulated analysis that very small reflections at the interface between the port and the transmission line will contribute a first-order effect of ripples in the extracted differential insertion loss. The ripples in the insertion loss will actually be amplified while only including a single-ended launch model in the presence of significant launch coupling. So, it is the full differential impedance profile (including coupling) that must be used in the launch model with de-embedding.

Step 3: Conversion of Two-Port Sij to Differential Smn11

For our demonstration we converted the measured two-port S_{ij} to differential one-port S-parameters, and apply the peeling method to differential S-parameters directly (using the 180 psec delay time). The S_{DD11} parameter gives us a bit more intuition. Even though it is acquired from single-ended two-port S-parameter measurements, S_{DD11} shows us how a differential signal would propagate, reflect off the short circuit, and return to a test port that is 100 +j0 Ohms. Assuming a perfect short circuit, the de-embedded S_{DD11} provides the round-trip loss and impedance mismatch effects (Fig. 12). The S_{DD11} phase is also important for the effective Dk test below, but is not shown in this plot.

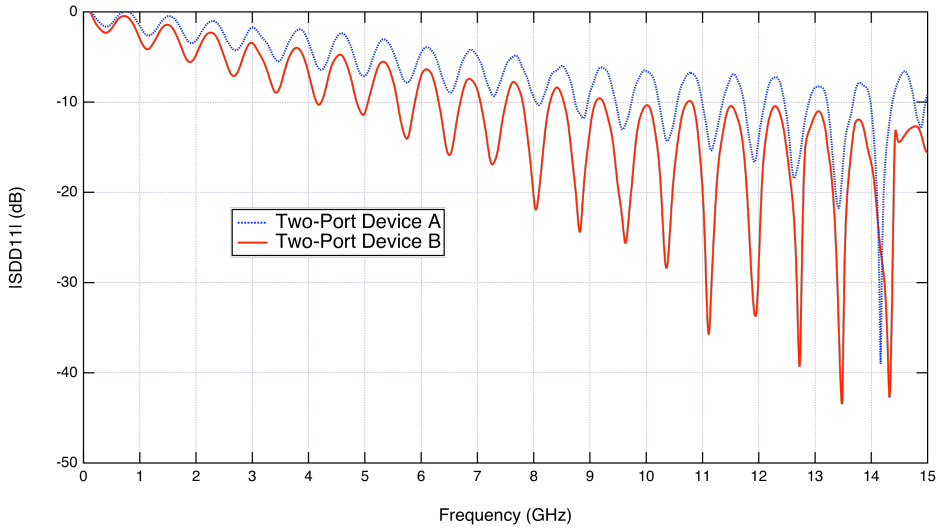

Fig. 12. $|S_{DD11}|$ of the SET2DIL-like test devices shown in Fig. 1. The behavior includes propagation loss effects (round trip), impedance mismatch between the network analyzer reference impedance and the characteristic impedance of the line, and artifacts of an imperfect differential short-circuit.

Step 4: Extracting Figure of Merit

Using the display of this S_{DD11} response in the time domain, the differential impedance of the pair and its uniformity can be directly measured. This impedance is also used to renormalize the differential port impedance and compute a smoother $|S_{DD11}|$. Since the characteristic impedance Z_0 of a lossy line is a complex function of frequency, normalizing by a single number will not "smooth" the mismatch of the entire $|S_{DD11}|$ function. In the figure below, we used a longer-time Z_0 measurement from the TDR profile, and this optimized the lower frequency portion of the curve (Fig. 13).

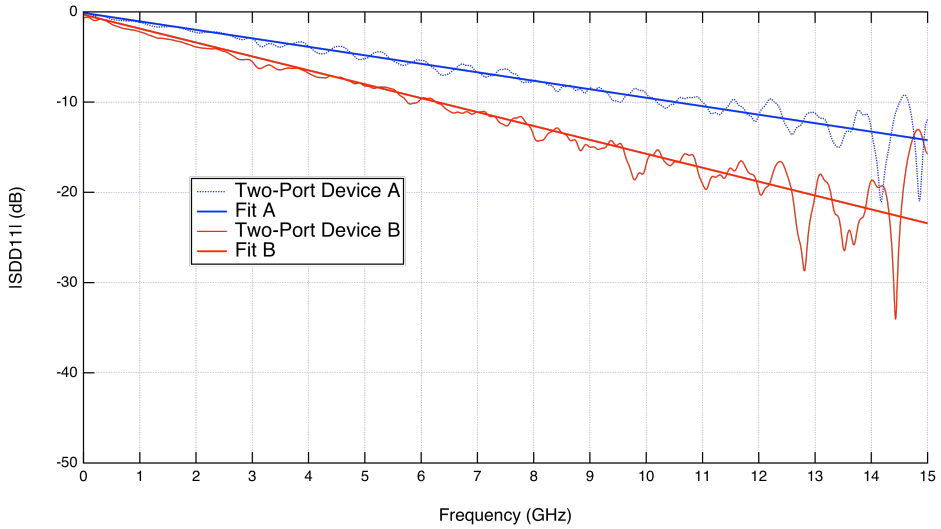

Fig. 13. $|S_{DD11}|$ *from two test coupons after renormalization to* Z_0.

We fit the renormalized $|S_{DD11}|$ to a generic curve for the response of signal propagation along a loss line. $S_{DD11} = \exp(-\gamma 2L)$, where $\gamma = \alpha + j\beta$ is the propagation factor of the signal, and 2L is the round trip length of the one-port SET2DIL line of length L.

The real part of the propagation factor gives us the total propagation loss, which is the basis for total loss production testing. Figure 14 shows the loss as a function of frequency for two different test coupons. As observed in many other studies, the loss curve (in dB/m) is has a nearly linear frequency slope at higher frequencies and a dispersive curve at lower frequencies (inducing a non-zero intercept).

Following the method of extracting Dk as shown in the Method section above, we use the phase of S_{DD11} to compute an effective Dk for the two-port test device and compare to those obtained from measurements of the matching four-port differential transmission line. Figure 15 shows values for effective Dk obtained directly from the S_{DD11} phase data, and the effective Dk obtained from S_{DD21} of the four-port differential line.

Success of the method is determined by comparing two-port extracted parameters with actual four-port S-parameters of a matching differential test line. In the loss and Dk cases we see very close agreement in loss (Fig. 14) and Dk (Fig. 15) when using repeatable pads and launches. It's important to realize that the two-port results are those obtained independently from our method and not at all fit or weighted by four-port measurements.

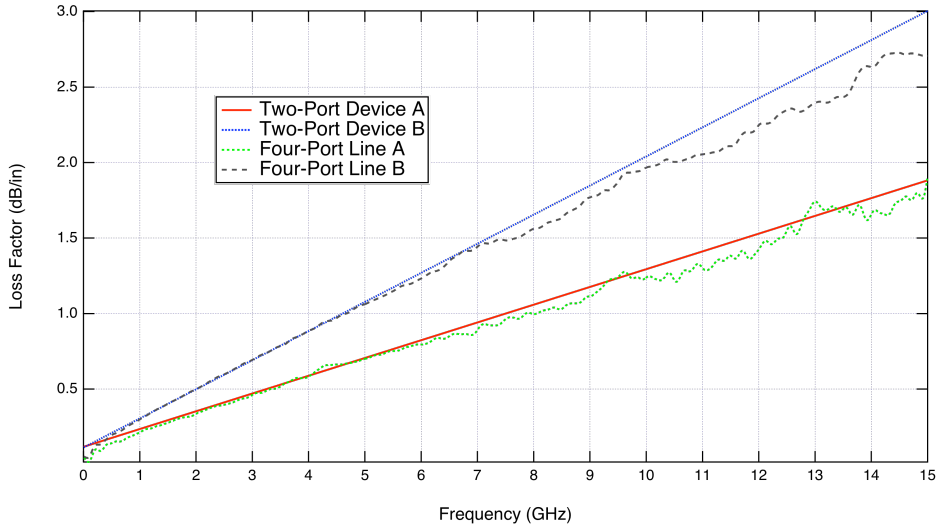

Fig. 14. The loss factor $\alpha(f)$ *for two test coupons from fitting the self-normalized* S_{DD11} *to a generic model, compared to the loss factor obtained directly from* S_{DD21} *of matching four-port lines.*

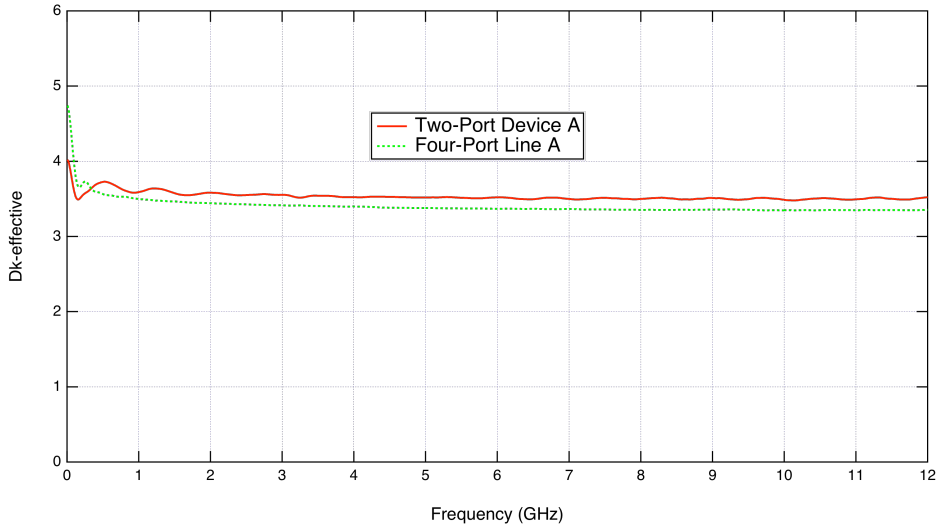

Fig. 15. Effective Dk from the phase of the self-normalized S_{DD11} *of the two-port test device and from the phase of* S_{DD21} *of the matching four-port line.*

We now have figures of merit that can be used to test the loss and phase propagation of signals on a fabricated coupon against criteria we imposed on our PCB fabricator for pass/fail assessment. And, we have an archive of the full two-port S-parameters for further analysis. Our final loss and Dk figures of merit do not include effects of fixture launch nor the effects of reflections due to the inevitable mismatch between the characteristic impedance of the line and the reference impedance of the network analyzer (or TDR) port. This gives us unambiguous characterizations for testing and comparisons.

Additionally, the loss factor curve $\alpha(f)$ allows the designer to compare directly the prediction of their CAD tool model of this line to frequency-dependent measurements of an actual implementation of the design. Differences can be identified. The causes may include an imperfect representation of the copper surface roughness [3] in the CAD model when the high-frequency losses are greater than expected while mid- and low-frequencies losses match. Causes may include non-uniform copper etching or adhesion profile when $\alpha(f)$ is not linear over broad bands.

In the process, we made an assessment of the differential characteristic impedance of the transmission line and can test Z_0 using the same test data and test equipment. Loss and Z_0 testing at the same time will help identify any mistakes made in the parameters used to describe the dielectric material or the width of the copper traces. For example, if Z_0 is within bounds, but loss is too large, it is likely copper resistance is the culprit (either in imperfect CAD parameters or limits in manufacturing). If, however, Z_0 is out of bounds, it could indicate the dielectric Dk and Df parameters are not in agreement with the engineering prediction.

Wait, there's more (more eating of the cake). By extracting the propagation factor from two-port S-parameter measurements, we also have the phase factor $\beta(f)$ function and the related phase velocity function $v_p(f)$. These too are dominated by the reactive components of transmission line (L and C instead of R and G) and can be used to compare predictions of propagation velocity in fabricated structures to models.

We end with a preview of testing the skew between the positive and negative lines in the differential device. The velocity in both lines may vary due to their location over a glass fiber bundle in the PCB dielectric or non-uniform copper etching. Loss and velocity may vary due to uniformity of copper roughness profile. To test for this, we look at the mixed mode S-parameter S_{CD11} or (S_{DC11}) and convert to the equivalent S_{CD21} to see mode conversion due to signal skew. The S_{CD21} provides a very sensitive measurement of how different the propagation is in one of the conductors relative to the other in the differential pair, and can tested against a threshold of tolerable delay skew or non-uniformity.

Figure 16 shows the S_{CD21} cross talk extracted from the SET2DIL-like test device compared to S_{CD21} measured on the matching four-port line. Again, we see remarkable agreement between data extracted from two-port test device to that expected from an actual differential transmission line of matching design.

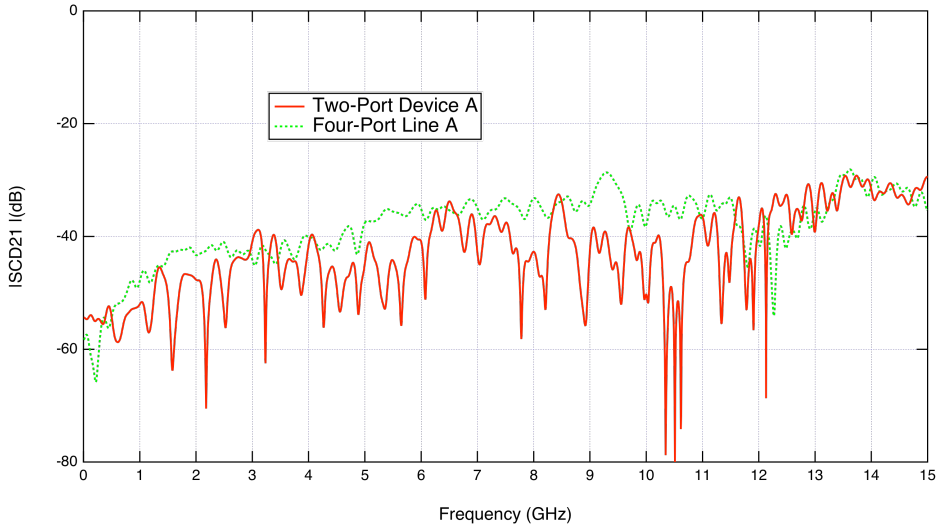

Fig. 16. $|S_{CD21}|$ *representing differential delay or loss skew.*

Conclusion

Two-port S-parameter measurements of simple production test coupons provide a wide suite of tests suitable for fabrication tracking. Those tests not only ensure that extreme performance specification are being met in production, but archiving the measurements and extracted transmission line parameters provide valuable engineering feedback to improve design models and to correlate design models to actual fabricated structures.

All of this information is available to the engineer and the production facility by acquiring two-port scattering parameter of simple test coupons, quickly. The success of this method is shown in the remarkable comparison to four port measurements of matching differential lines (slower measurements).

Systems based on time-domain network analyzers make this possible through the use of coupon fixtures suitable for the rugged production environment, but precise enough for the OEM development lab. The ability to acquire the engineering information using a measurements and methods common to both the OEM and the production provides a clear opportunity to improve design with feedback from manufactured boards.

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